32 Bit Clock Sequencer

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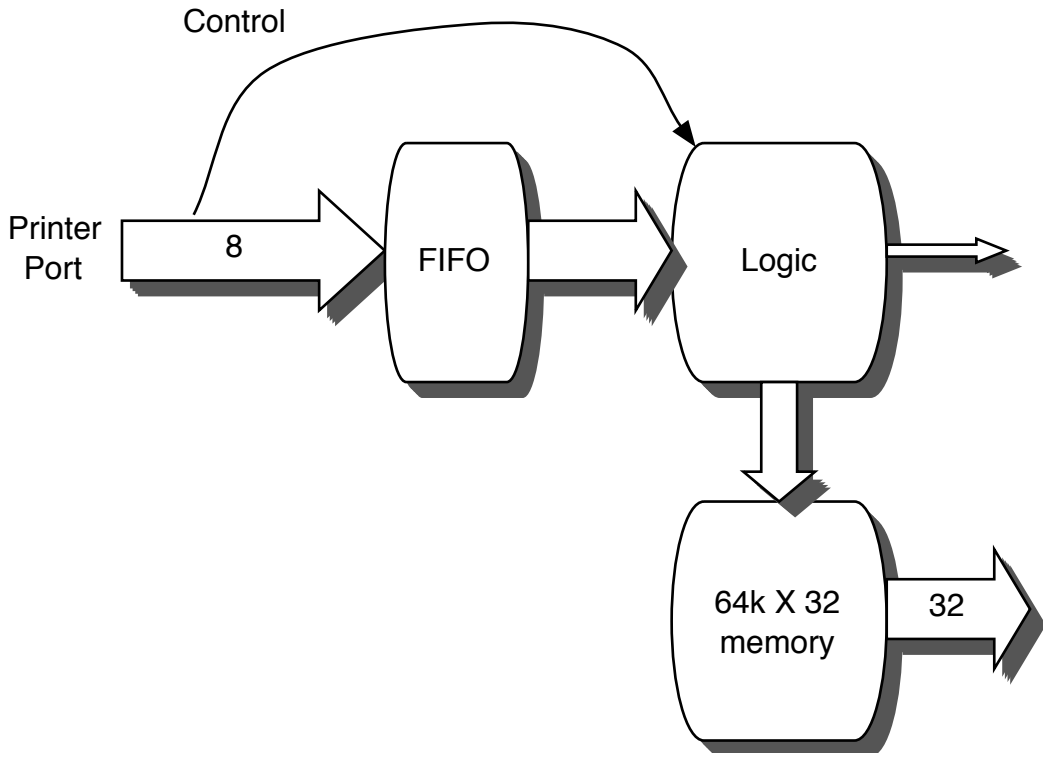
The sequencer generates clock sequences from memory on command.



Control port:

The control port is a standard parallel printer port. There's a good tutorial on these at:

http://et.nmsu.edu/~etti/fall96/computer/printer/printer.html

Registers:

The Sequence Length Register (SLR) is a 16 bit register that controls the number of 32 bit words generated by a single sequencer command. The number is one more than the value in this register: a value of 0 means a sequence is a single word.

The Clock Divider Register (CDR) is an 8 bit register that controls the number of master clock steps per output word. The number is one more than the value in this register: a value of zero means there's one master clock cycle per output word.

Byte ordering in the control stream:

Bytes within a multi-byte word are in "littleendian" order, least significant byte first.

Initialization:

If "Select Input" is asserted (low) and "Initialize Printer" is asserted (high), the sequencer logic is reset. Deasserting "Initialize Printer" places the sequencer in the initialization state. In this state, the logic accepts:

SLR value (2 bytes)
CDR value (1 byte)
Memory contents (256K bytes)

Once the memory is loaded, the sequencer enters the idle state.

Operation:

A command contains 6 memory block address bits, and 10 repeat count bits. Once a command is received, the sequencer leaves the idle state and enters the active state. In this state, it emits 32 bit words from memory, starting from the word address whose 6 MSB's are the memory block address from the command, and whose 10 LSB's are zero. The SLR determines the number of words emitted in one repetition. The repeat count in the command determines the number of times the sequence is repeated (again, a value of zero means once). Each time the sequence is repeated, the starting memory address is reset. Each repetition therefore produces identical output.

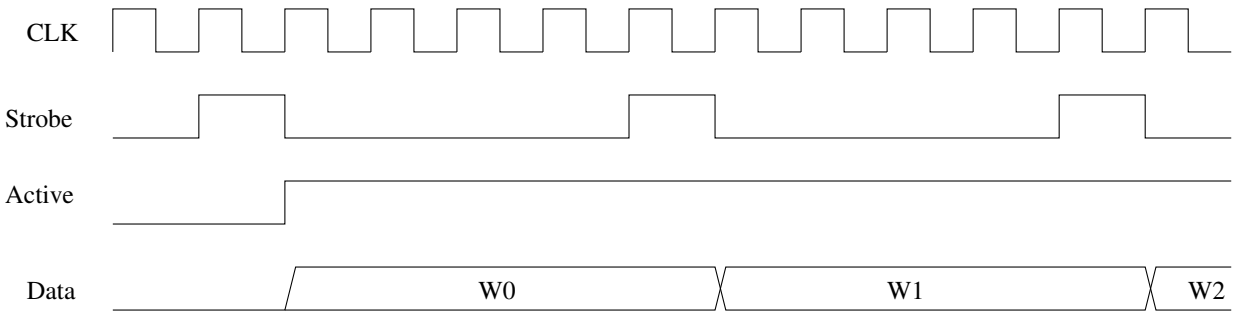
While this is happening, the sequencer is ready to accept more commands into its FIFO. When a command is finished, the sequencer should seamlessly start the next command if available. If no command is available, the sequencer should enter the idle state.

Outputs:

CLK+	Buffered master clock
CLK-	Buffered master clock
Strobe+	Data strobe
Strobe-	Data strobe
Active	Actively generating data
Reset	Buffered "Initialize Printer"
Data	32 data lines

The CLK and Strobe outputs are fast, so they are differential. Resetting the sequencer drives the Data outputs low. In the idle state, the data outputs hold their most recent value. The following timing diagram shows the transition from an initial

idle state to the active state. In this case, the CDR is assumed to hold the value 4:



Requirements:

Master clock of 30 MHz.
Handle at least 100,000 commands/s.
FIFO at least 64 bytes deep.