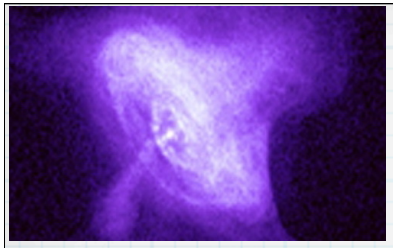
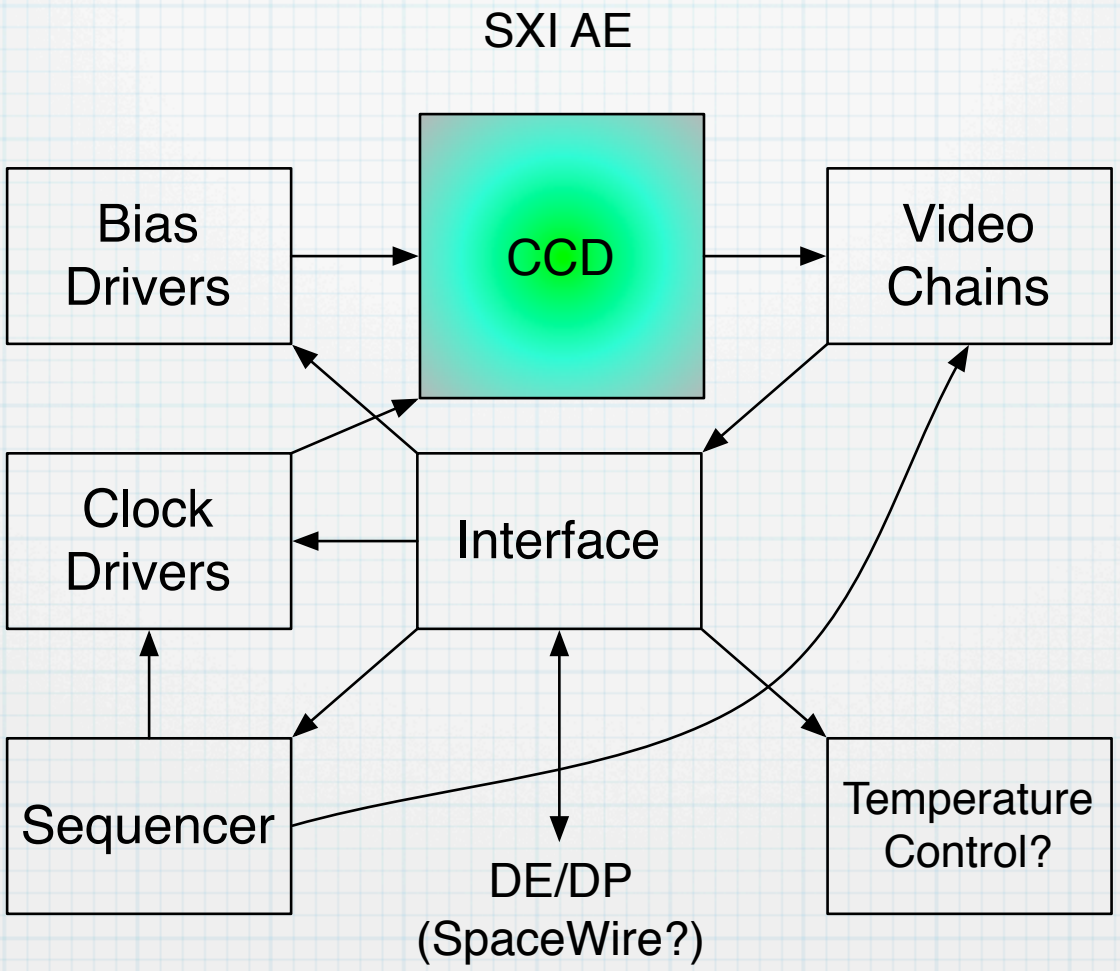
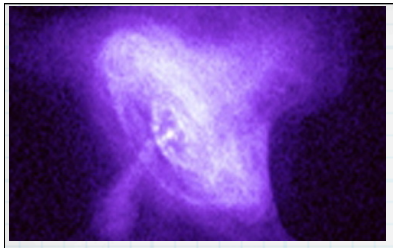


SXI Electronics Development at Noqsi Aerospace

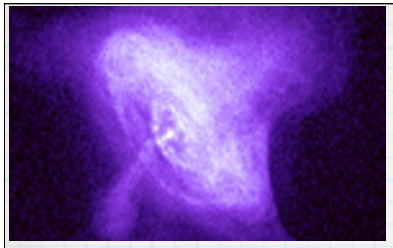




Design Practices

Use ISAS style.

- Be conservative but not dogmatic.
- Protect against CMOS SEL with current limits.
- Protect against SEU operationally with periodic resets and reinitialization.
- Avionics parts when possible.
- Meet needs of instrument first.
- Assume instrument receives regulated (“2ry”) power.



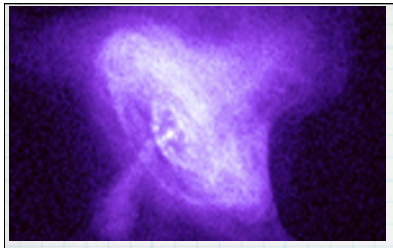
Clock Drivers

Requirements:

- ±15 V max swing
  - (large)
- 1MHz pixel rate
  - (for serials: what about parallel clocks?)
- Parts procurable in Japan
- Handle two phase CCD's up to 25 cm^2

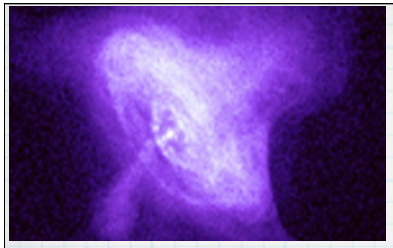
Goals:

- Low power
- High reliability

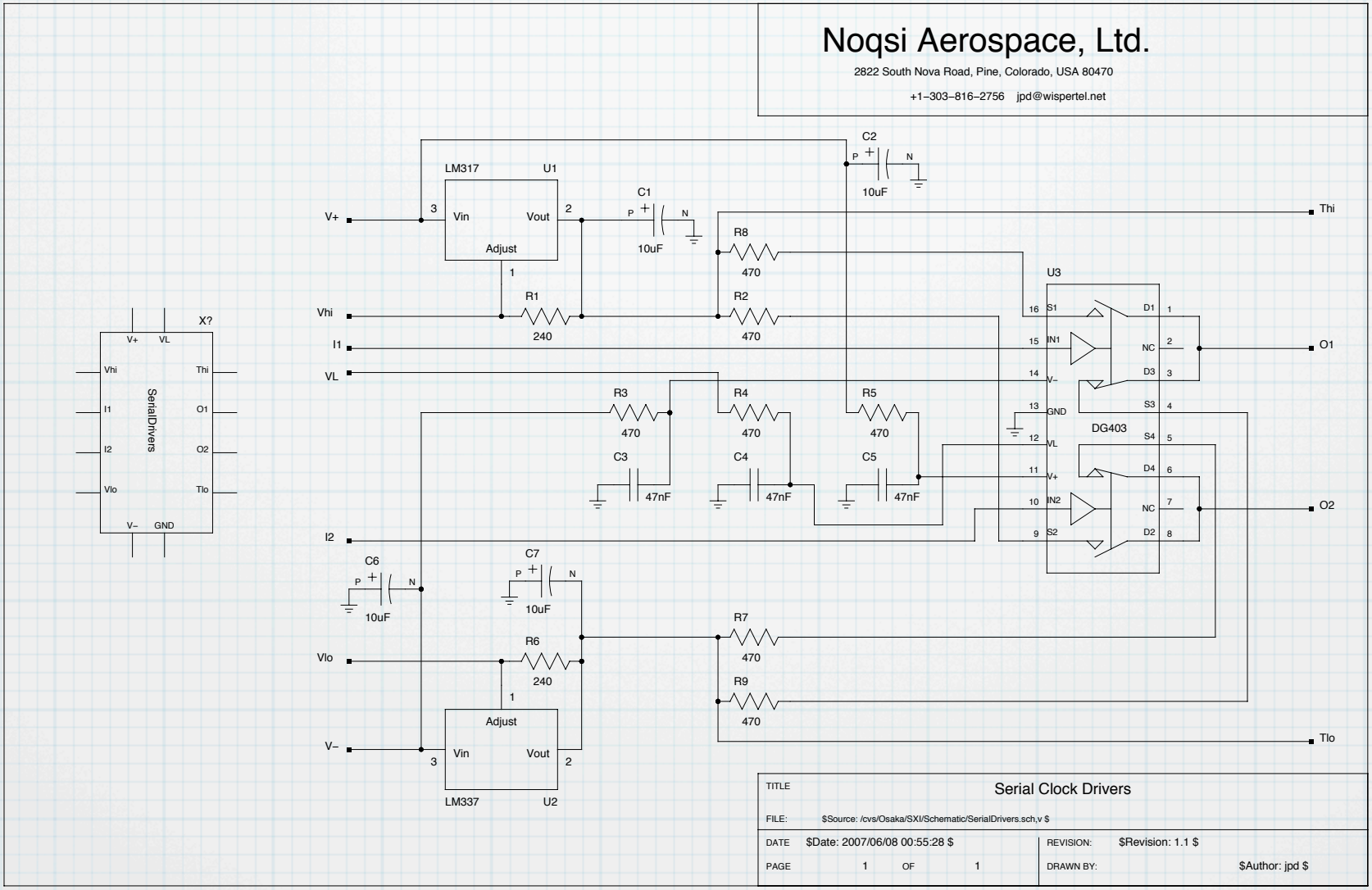


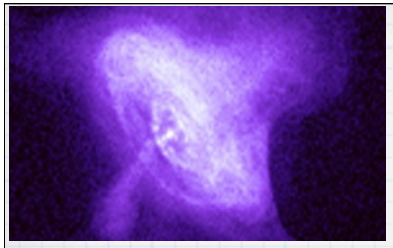
Design Parameters

- Capacitances?
  - Guess 75 nF for each parallel phase.
  - Guess 200 pF (including cable) for each serial phase and reset clock.
- How much peak power available for parallel clocks?
- Assume radiation environment similar to ASCA and Suzaku.
  - Moderate dose.
  - SEU likely. SEL possible.

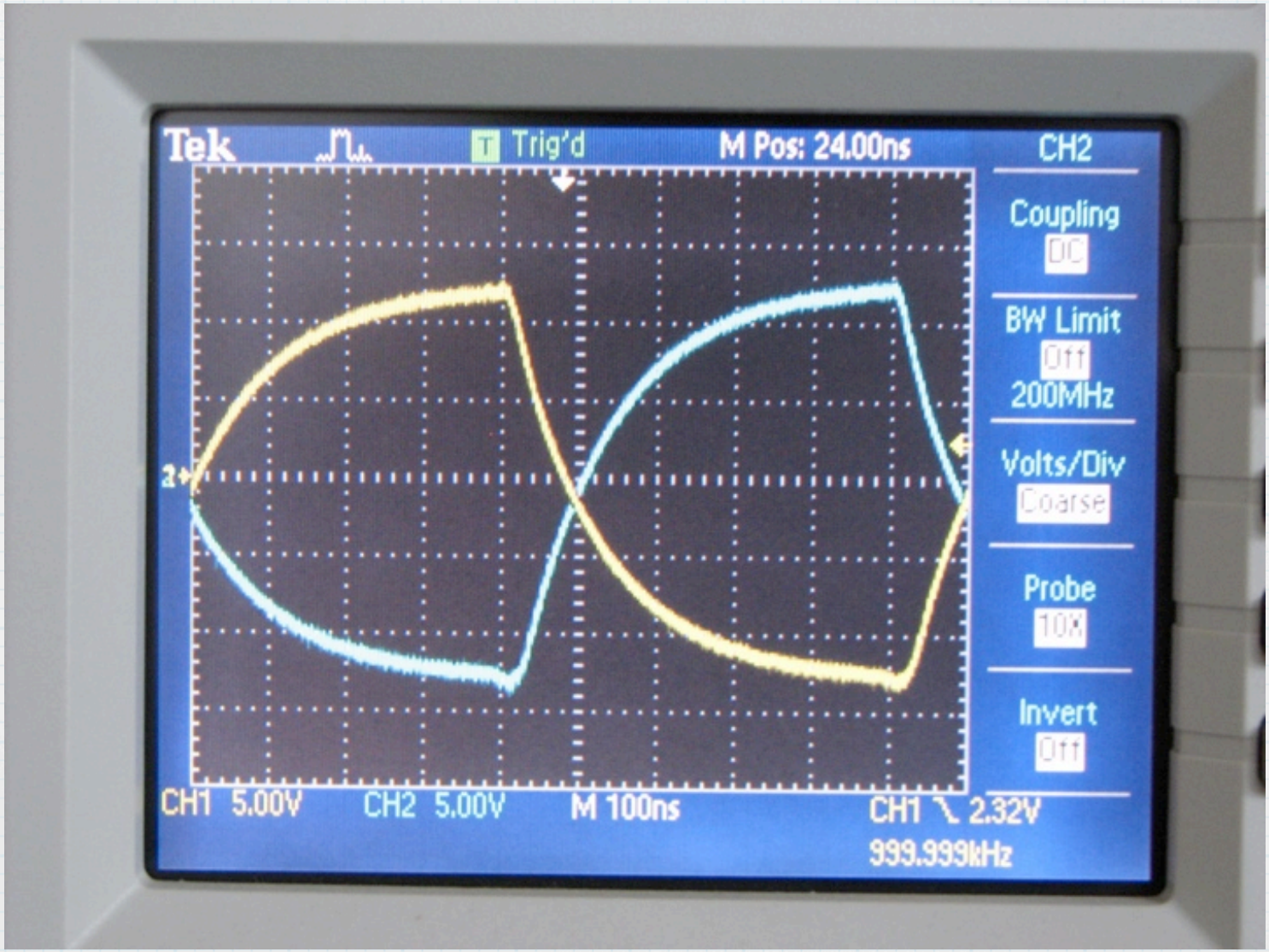


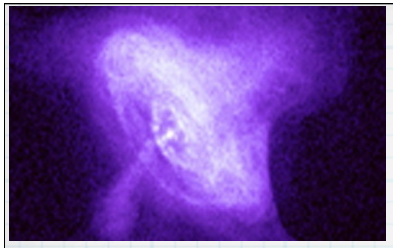
Low capacitance drivers (serial and reset)





Operation at 1 MHz, 200 pF loads





Power Consumption

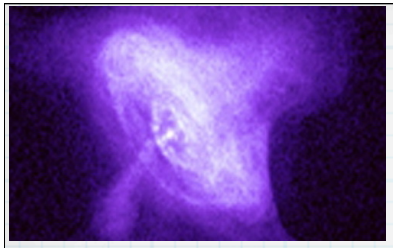
1 MHz, ±18V supplies, ±12V clocks,

200 pF loads

- Static overhead: 180 mW (LM317L and LM337L)
- Dynamic overhead: 130 mW (DG403)
- Power due to load current: 350 mW

Possible improvements

- More efficient regulators
- Reduced voltage requirements



Parallel Clock Driver

Noqsi Aerospace, Ltd.

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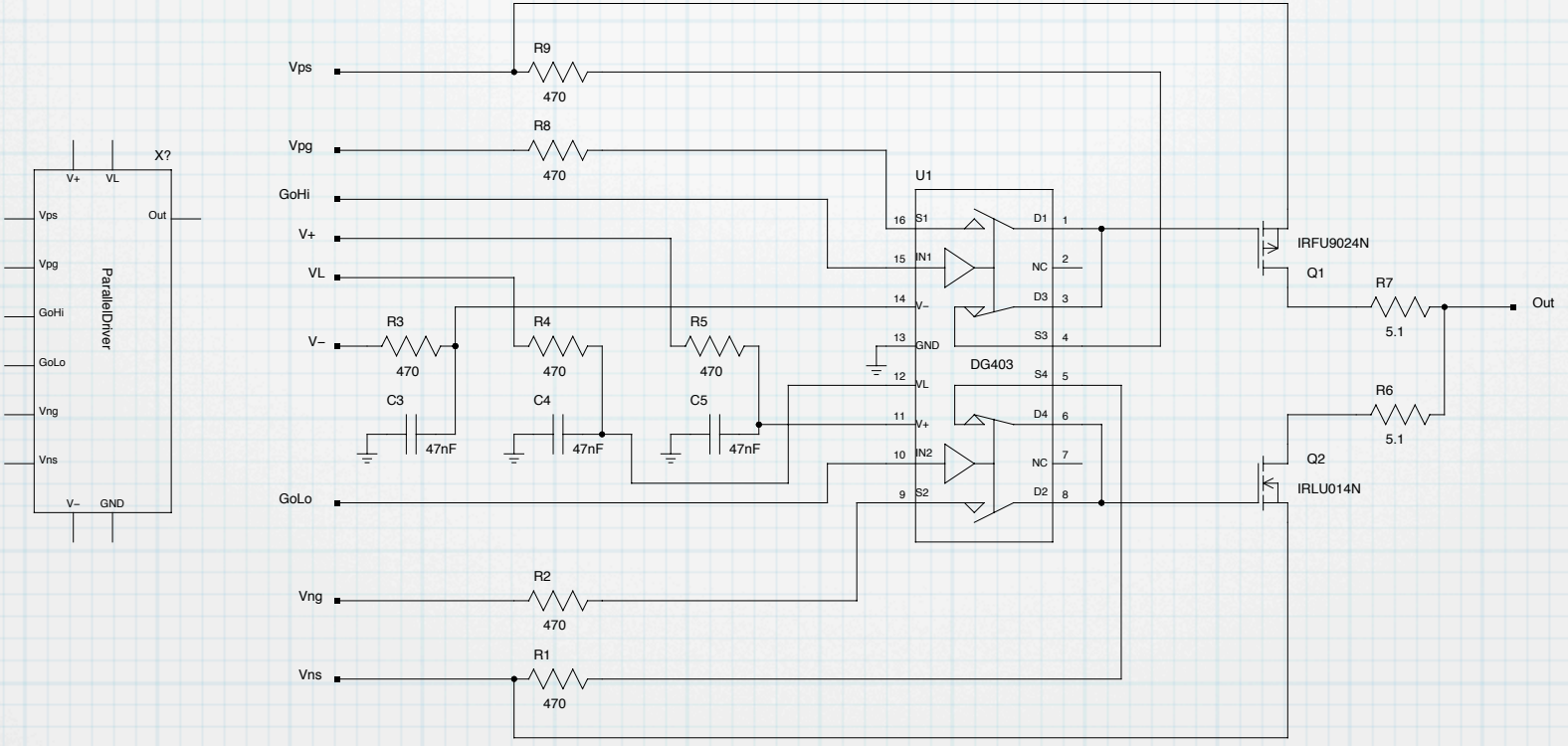
+1–303–816–2756 jpd@wispertel.net



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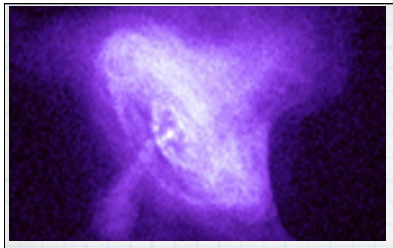
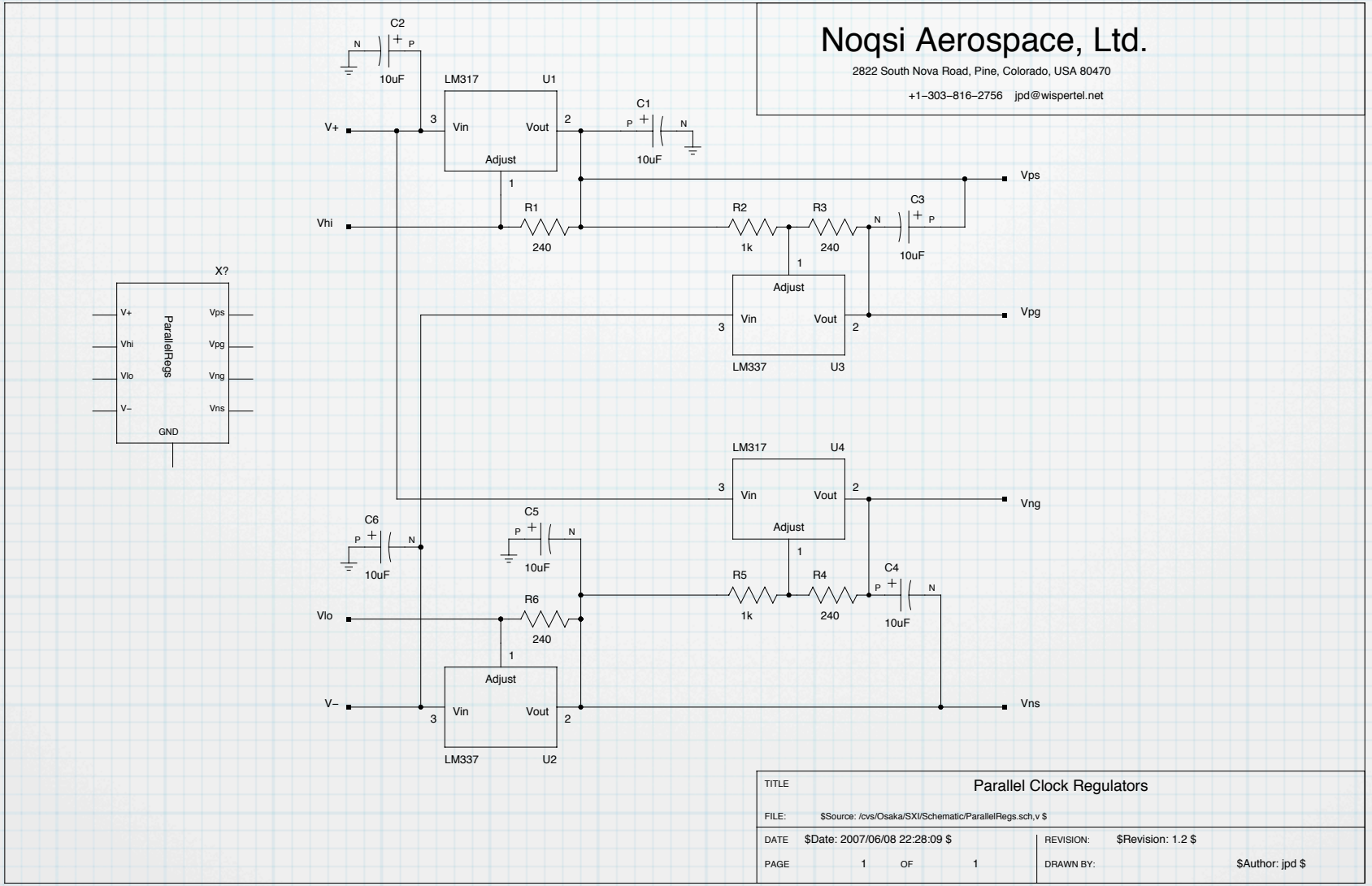
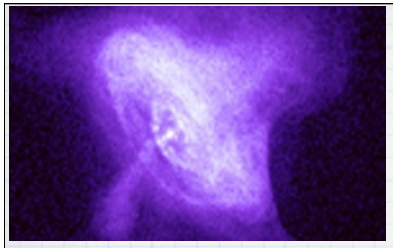
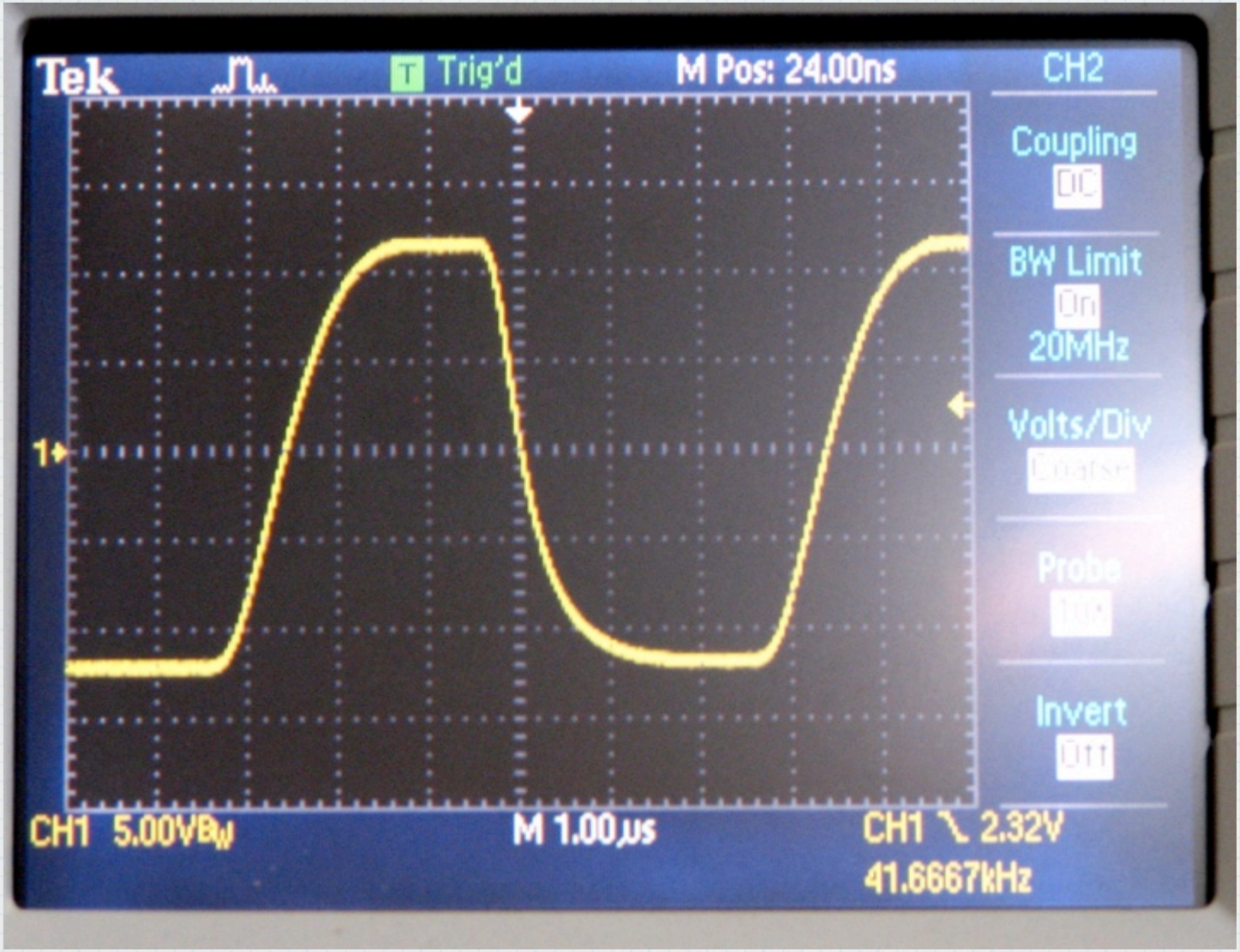


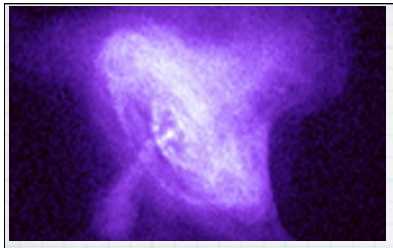
Regulators for Parallel Clocks





Operation at 167 kHz, 78 nF load





Power Consumption

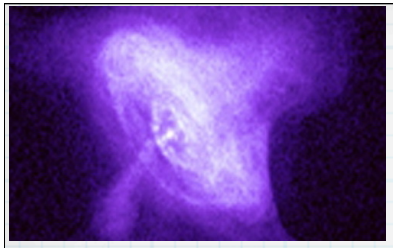
167 kHz peak, 43 kHz average, ±18V supplies, ±12V clocks, 78 nF load

Regulators: 540 mW static

- Can serve four drivers

Driver dynamic power (one driver):

- 2.8 W average
- 11 W peak
- 99% of this is due to load



Discussion of clock power

CCD clock power scales unfavorably with increasing telescope focal length

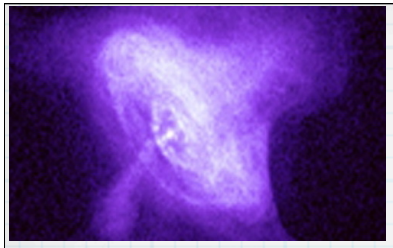
- See SPIE 6266-56 from 2006

Two phase CCD's need large swings

- Clock power scales as CV^2

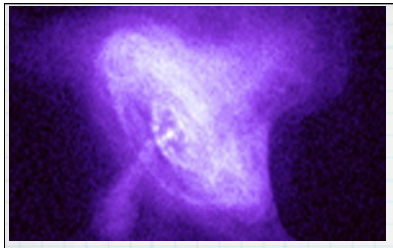
Need to refine requirements versus power

- Available power?
- Frame store time (streaking)?
- Fast modes and pixel summation?
- Reduced clock swings?



Digital to analog conversion

- Two possible approaches:
  - CMOS resistive ladder DAC's (like ASCA, Suzaku)
    - This technology tends to be somewhat sensitive to radiation dose.
    - For recent projects, I've used the AD5621 (tiny, micropower).
  - Serial oversampling (delta sigma) DAC's (like Suzaku TEC controller).
    - Somewhat more complicated, but most complication is in FPGA.
    - Need extra analog filtration, but that's not difficult.



DAC output amplifier

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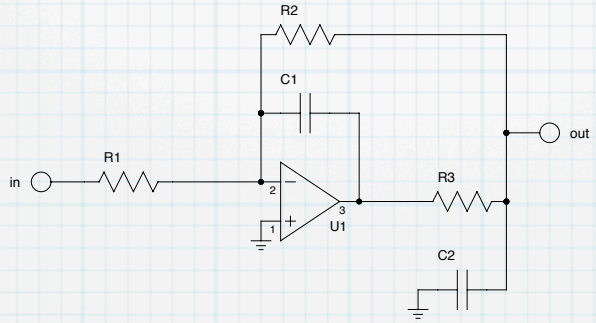
2822 South Nova Road, Pine, Colorado, USA 80470

+1–303–816–2756 jpd@wispertel.net



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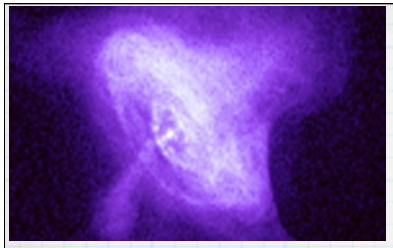
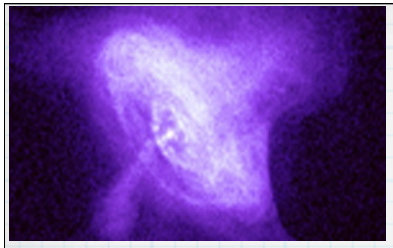


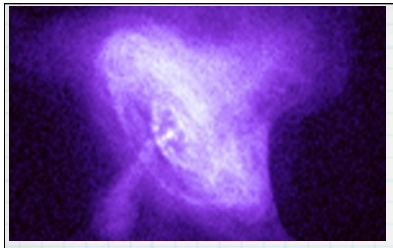
DAC output amplifier

- Regardless of DAC technology, need amplifier from ~3V DAC output
  - Potential noise introduction path
    - Bandwidth limited
    - Capacitive output
  - Power very sensitive to voltage
    - For supply span <30V, use OP220 (as on ASCA, Suzaku).
      - But need span of ~36V for ±15V clock range.
    - For larger span, fewer choices. OP77 is maybe best, but takes 20X the current of OP220!



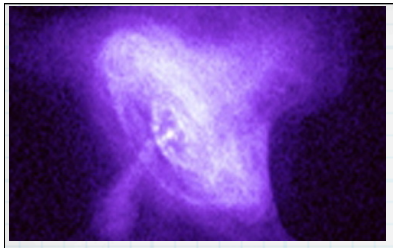
Bias Drivers

- Requirements
  - Output to +25V
  - Most very low current
    - Can use DAC output amplifiers directly.
  - How much current needed for CCD charge amplifier drains?
- Can use OP220 here to save power.



Video Chains

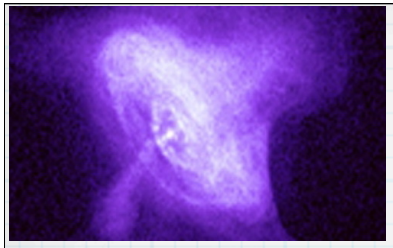
- ASIC based on MD01 is possible
  - Very small, energy efficient
  - No “dragon’s teeth”, excellent DNL
- Backup plan: Suzaku-like chains
  - Fast, low power opamps and switches make this approach much easier than 10 years ago
  - Some “dragon’s teeth” from ADC DNL.
- Need requirements, CCD specs



Sequencer

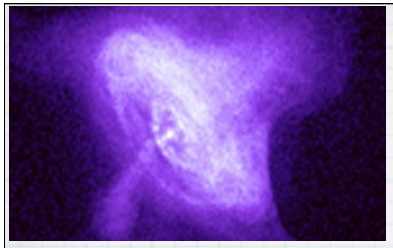
Requirements?

- Lots of ways to do this:
  - ASCA-like single level state machine
  - Suzaku-like multilevel microcode
  - Mix and match features from those
  - RAM/Flash FPGA's make state machine approach flexible
- How much bandwidth/latency to DE/DP?
  - On ASCA, DE issued a sequencer command every pixel
  - Suzaku DE doesn't work so hard
- Who designs this?



Temperature Control

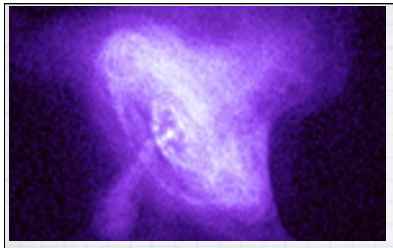
- Is this required?
  - And what are the requirements?
- If so, who designs this?
  - Thermal, mechanical, electrical design are all closely connected here.



Interface

FPGA to present AE interface to DE/DP?

- SpaceWire?
- Other requirements?
- Who will design this?



Final Questions

When?

- Schedule?
- Resource budgets (power, mass, 円, etc.)?

System

- System engineering ISAS-like?
- Preferred parts?
- Preferred interfaces?