Designer's notebook for NeXT SXI CCD System

5/26/07 jpd

Clock Driver Requirements:

±15V max swing
1 MHz pixel rate

Parts procurable in Japan. I don't think this will be a problem: I don't like to use exotic parts.

CCD's up to 25 cm^2, including frame store. Two phase devices.

Goals (no quantitative requirement yet):

Low power consumption.

High reliability in a moderate radiation space environment (low altitude, medium inclination). Part of this goes beyond the applied physics: must convince reviewers. A difficulty is that I don't know what the review culture for NeXT will be.

Design parameters :

No capacitance spec, guess 75 nF per phase for parallels for now.

Guess 200 pF per phase for serials and reset, including cable capacitance.

Design practices:

Protect all CMOS against latchup with current limiters or circuit breakers. Current limits on on other technologies as practical. Remember, one advantage of having these is you protect the circuit against hidden damage due to short circuits or power sequencing violations in testing.

Don't worry about other radiation-induced upsets too much: we can reset and/or power cycle the instrument to clear these. Rates are low even for soft technologies in this kind of orbit.

Technology:

Try to make it possible to use avionics grade versions of commercial parts. But don't be stupid, the needs of the instrument come first. Keep stresses low, margins adequate, high quality components will be reliable. Try to avoid specialized parts made only for space: these are hard to procure and tend to exhibit unpredictable behaviors in application circuits.

Radiation dose moderate, guessing <3k rad over several years. Still, radiation data a plus for selection. If we need to test a part, do it: it's expensive, but not as expensive as distorting the engineering by using parts that don't match other requirements well.

Ideas:

Use Maxim DG403 for level translation. 100 mA peak current yields 0.5V/ns with 200 pF load, good enough for low capacitance drivers. Could use both switch pairs in a package in parallel to reduce stress. DG403 has low static power, avionics grade available.

For fast high capacitance drivers, use power MOSFETs. Rad hard IRHF57034 and IRHY59703CM can handle large surges (but note my suspicion of such specialized parts above. And are they procurable in Japan?). Commercial grade transistors have better specs except radiation, and are probably rad hard enough (better margins in other areas). Don't need to decide today. But do we need 1 MHz parallels?

For a first prototype, use LM317/337 regulators (low power or regular versions) driven by op amps as clock regulators. Conservative, rugged, easy to obtain. Not the most efficient (5 mA minimum load is the main issue), but if power consumption too high, we can look for more efficient similar devices.

High-voltage low-power op amps are difficult to find. OP77 is 44V, good margins with the 36V span we probably need to achieve ±15V swings, but 2mA quiescent is a bit high. Later, if we can reduce the ±15V requirement we can save on power by revisiting component selection (and fCV^2 power will go down also).

Minimize energy dissipation in transistors. Resistors more rugged.

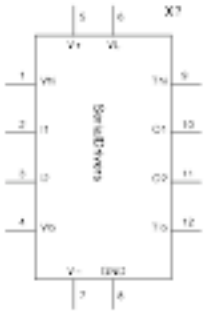
5/27/07 jpd

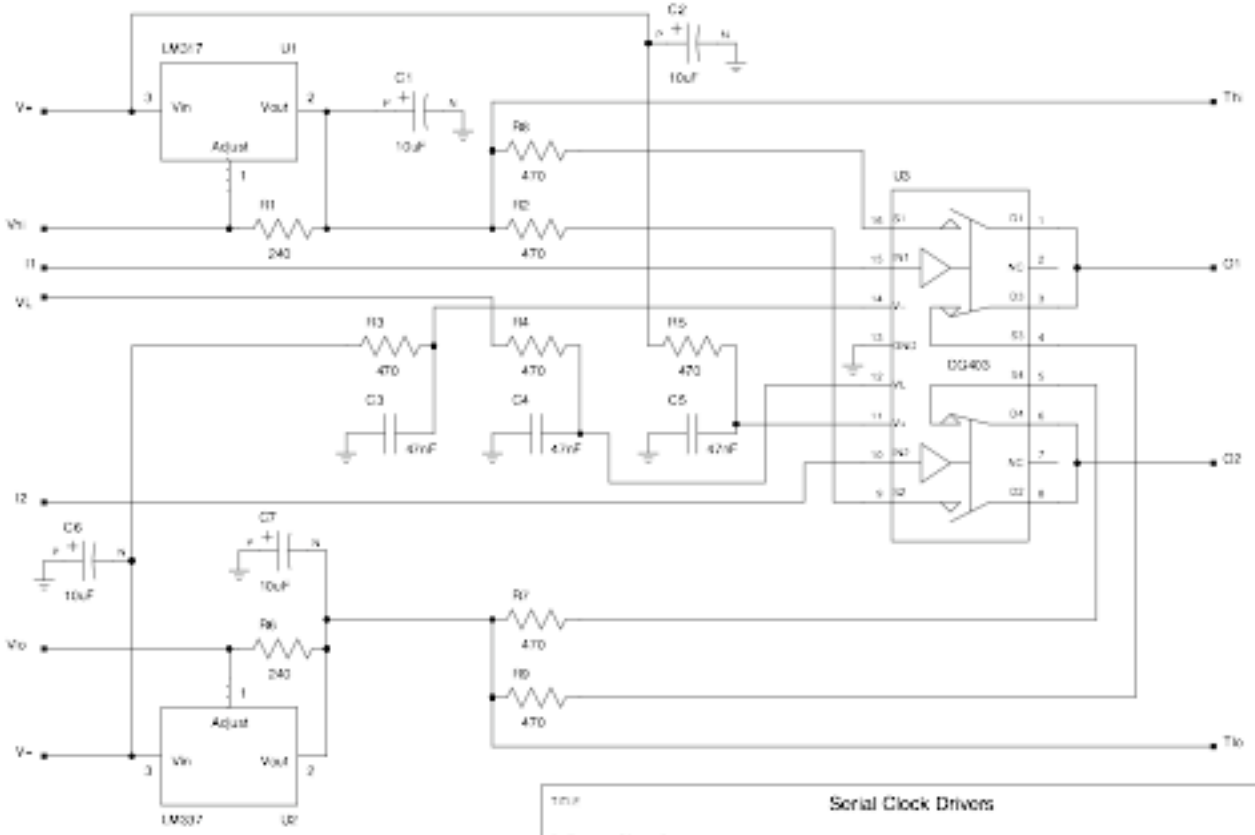
Serial clock driver block, first draft for PPM (pre-protomodel).

Noqsi Aerospace, Ltd.

2822 South Nova Road, Pine, Colorado, USA, 80470

+1-303-816-2756 jpd@noqsi.net





TITLE:	Serial Clock Drivers		
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Use 470 ohm, 1W resistors for current limiting. With 18V supplies, they'll dissipate 690 mW, max. That should be enough margin for something intended to handle rare faults (and I hope we can reduce the supplies). R4 is on 5V, so it can be 0.1W. In addition to static current limiting, R2, R7, R8, and R9 limit switching surges to 64 mA for 30V swings, sufficient margin for a part (U3, DG403) rated for 100 mA surges of much longer duration than we'll have here.

Inputs:

V+	Positive rail, 2V above max clock level, 18V maximum.
V-	Negative rail, 2V below min clock level, -18V minimum.
VL	Logic power, 5V nominal.
GND	Ground.
Vhi	High clock level will be 1.25V above this. Driver must sink 5 mA.
Vlo	Low clock level will be 1.25V below this. Driver must source 5 mA.
I1	Logic input to driver 1.
I2	Logic input to driver 2.

Outputs:

Thi	High clock level monitor output for housekeeping.
Tlo	Low clock level monitor output for housekeeping.
O1	Clock output 1.
O2	Clock output 2.

Logic is positive: a high level on the input produces a high level on the corresponding output. High threshold is <2.4V, so 3-5V CMOS levels OK.

5/28/07 jpd

Parallel clocks. If we assume 75 nF for each set of gates, 30V swings, 36V power, then the dynamic energy to clock a single set one cycle (C*Vswing*Vpower) is about 80 μJ (assuming no other dynamic losses in the drivers). There are four sets of parallel gates (two phases, imaging area and frame store), so it takes about 320 μJ to do one cycle of frame transfer, 320 mJ to do 1000 transfers.

Assuming 50% efficiency of the drivers, this doubles to 640 mJ. If we read the CCD out at two frames/second, that's 1.28W of average power required to do frame transfers (and 0.64W for the transfers to serial). But the real problem is peak power: if we take 5% of the readout cycle for frame store (and therefore misplace 5% of photons in the image), the frame store operation will require a surge of 25.6W for these parameters. That's getting difficult for a power supply.

The result is that the speed of the parallel clocks will be restricted by the available surge power.

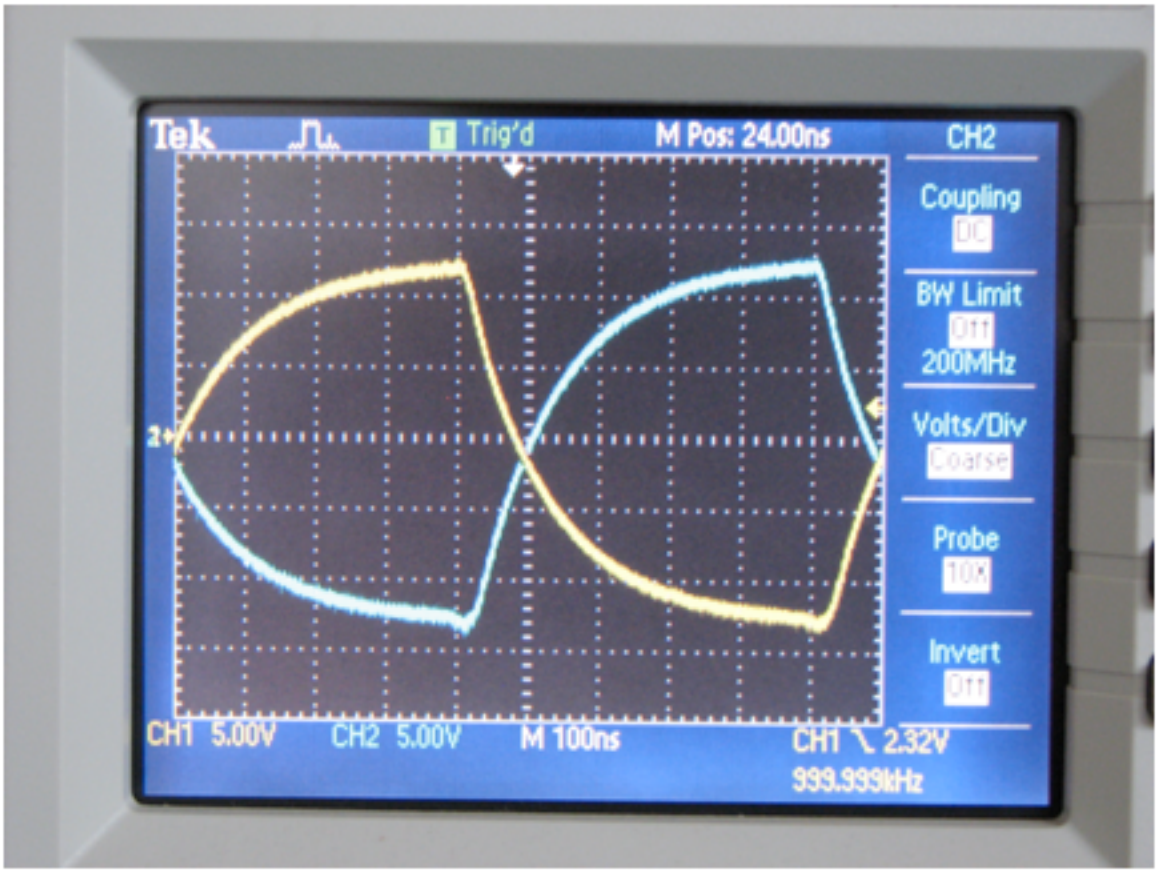
This issues will also limit pixel summation and continuous clocking modes.

It is important to understand what the magnitude of available surge power from the power supply will be. The capacitance of the parallel gates is also a critical parameter. Any reduction in the clock swing required will help here, too.

5/30/07 jpd

PPM serial clock first tests.

1 MHz, 200 pF loads, ±12V levels, ±18V analog supplies:



Looks good.

Power consumption:

Static overhead: 180 mW (LM317L and LM337L)
Dynamic overhead: 130 mW (DG403)
Power due to load current: 350 mW
Total: 660 mW

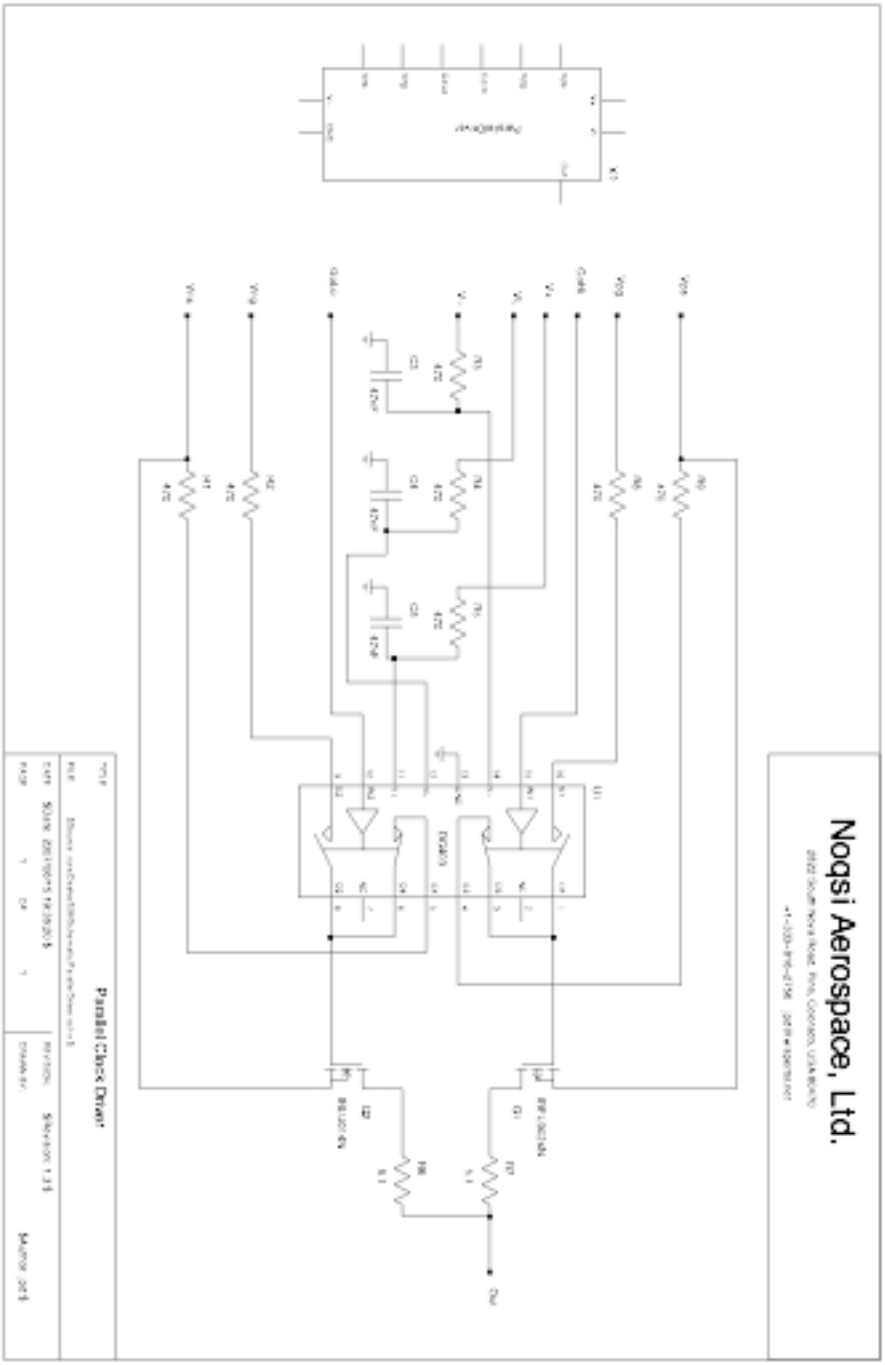
Given the requirements, this is reasonable. I could possibly reduce the static power somewhat by choosing different regulators, but static power is <30% of the total. The LM317L and LM337L are otherwise conservative choices. I don't see any other opportunities for power reduction for the given requirements. I could double the capacitive drive or cut the rise/fall times in half by using both channels in a DG403 to drive a single clock. For two clocks, that would increase power by 130 mW. So, pending review and refinement of requirements, this part of the design is done for now.

6/15/07 jpd

Parallel drivers.

These need a lot of drive for the high capacitance (estimated 75 nF per phase). While the DG403 makes a good level translator here, it doesn't have the current capacity to drive 75 nF at a reasonable speed: we need to boost its current with external transistors. This has the nice additional effect of separating the high current circuitry (difficult to protect against latchup) from the CMOS, although we will still have to worry about CMOS latchup causing dangerous drive conditions on the transistor inputs.

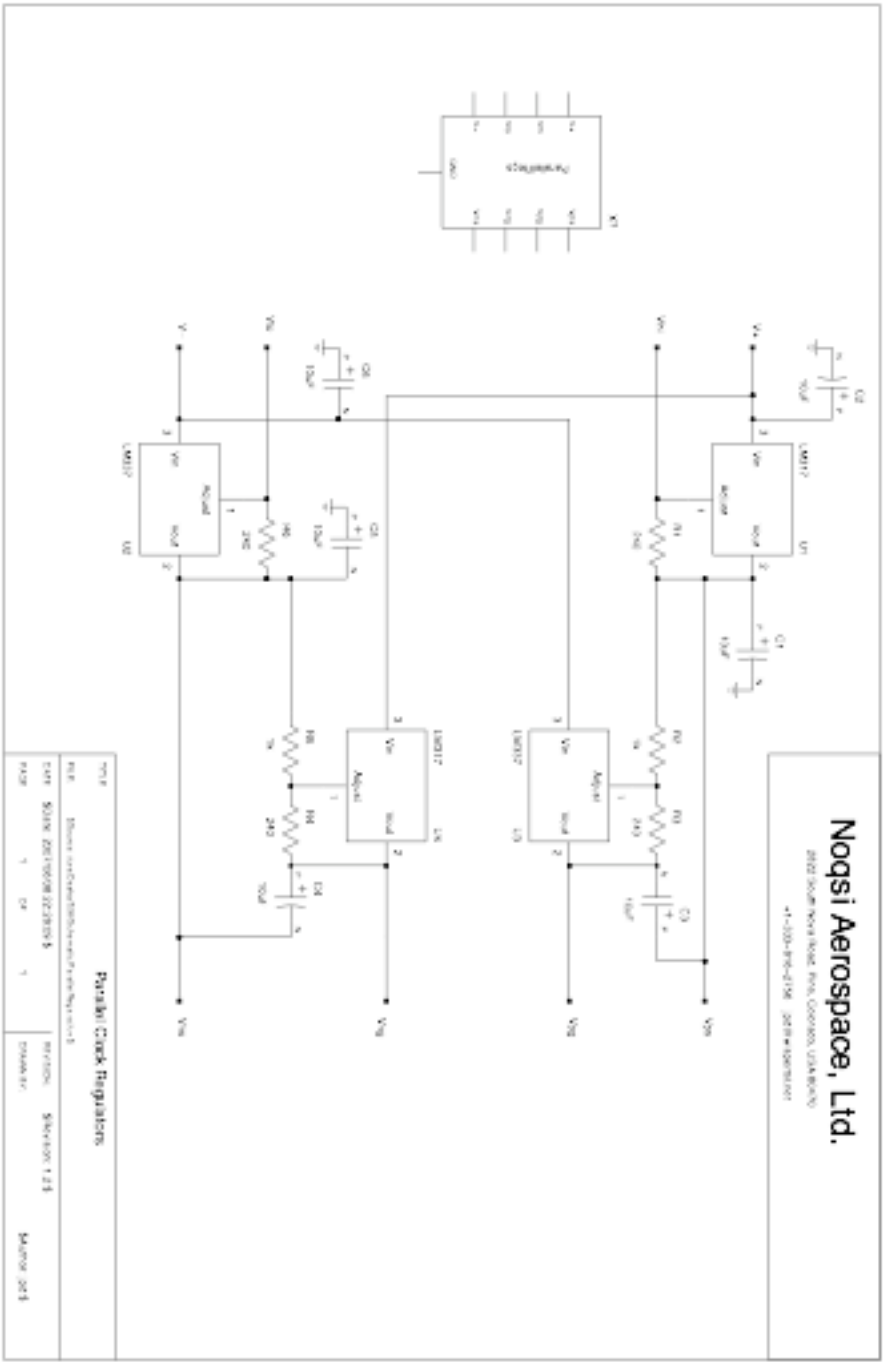
Here's my current schematic:



This drives just a single clock: four of these will be needed to drive both pairs of parallel clocks for one CCD. The logic inputs GoHi and GoLo are separate to allow logic to prevent large dynamic currents from the fact that it takes this circuit ~1μs to turn the drive transistors off. GoHi and GoLo should never be high at the same time, and the drive logic should also allow >1μs after driving one low before driving the other high.

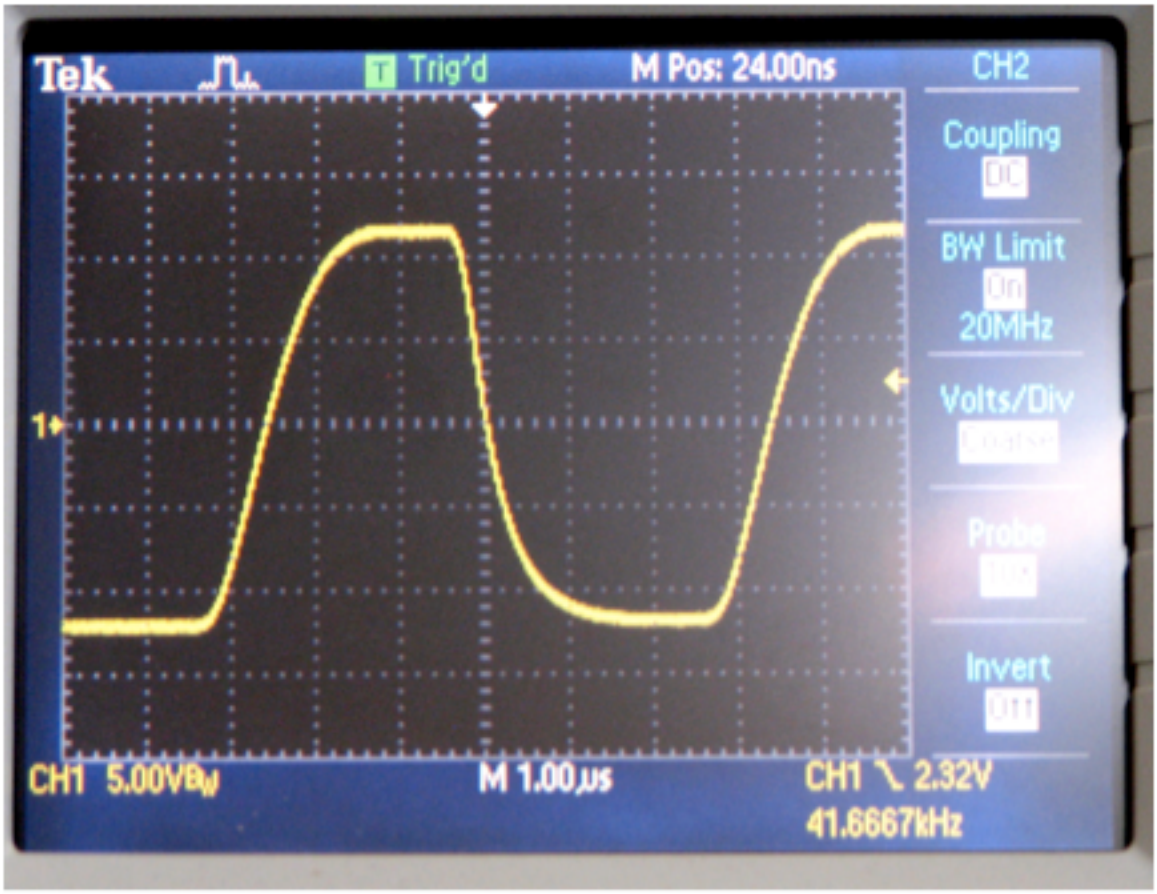
R6 and R7 are there to dissipate the capacitive energy, helping to keep Q1 and Q2 cool. The other resistors protect the DG403 against destructive latchup and other fault conditions.

This circuit needs regulators not only for the CCD clock levels, but also for the gate drive levels: the MOSFETs can only handle 20V on their gates:



One of these regulator sets could serve four drivers.

Here's a photo of a test at one cycle/(6 μs), ±12V swing, 78 nF load:



Note that the scope says it's 41.6667 kHz because the clocking program was 1000 cycles in 6 ms followed by 18 ms idle time. At 167 kHz, components get very hot when clocking continuously.

The regulators consume ~540 mW of static power. Dynamic power is ~2.8W average, ~11W peak for these test conditions for this single driver. Multiply dynamic power by 4 for a complete set of four drivers driving one CCD.

Only about 1% of the dynamic power goes to operating the driver itself: the rest is just charging and discharging the load capacitance.

6/19/07 jpd

Thinking about controlling the regulators.

What do we want to use for DACs? For the Suzaku XIS we used two kinds:

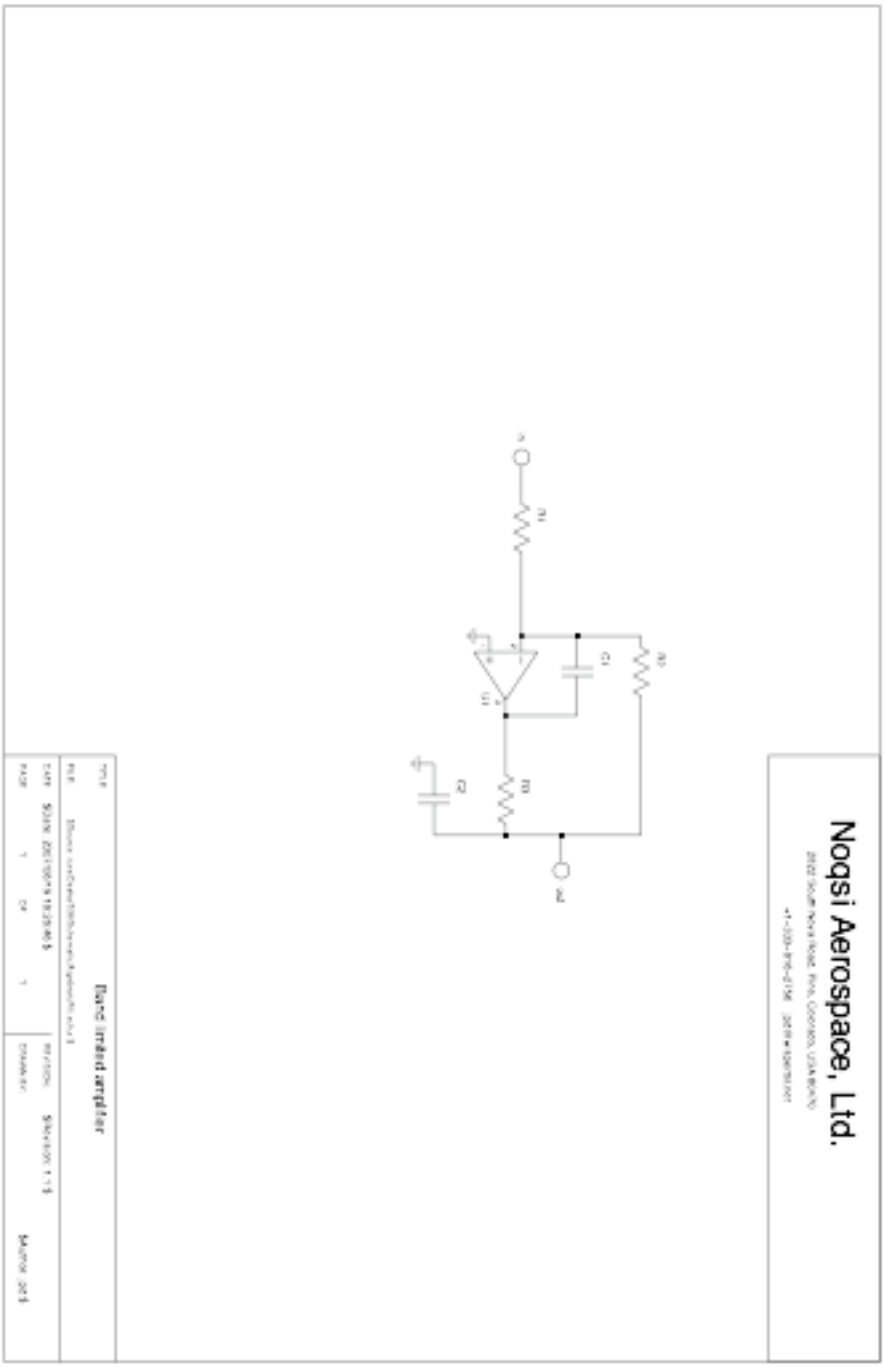
1. CMOS resistive ladder devices for clock and bias control.
2. Serial averaging (first order delta-sigma) circuits in FPGA for focal plane temperature regulation.

I've been using the AD5621 resistive ladder DAC in recent projects. It's tiny, takes very little power, and is easy to interface: probably a good choice. However, I don't know anything about its radiation tolerance. This isn't a difficult orbit for radiation, so it's probably OK, but we may want to check.

On the other hand, we'll probably use some kind of FPGA, and it can implement delta-sigma DACs at the cost of extra filtering circuitry.

The resistive ladder approach is perhaps slightly easier to design, while the FPGA approach slightly reduces radiation tolerance concerns. They are both low in power and compact. Something to think about.

In either case, the DAC/amplifier/regulator chain is a potential path for noise to get to the CCD. I like to restrict the bandwidth here to minimize the (difficult to analyze) potential for noise injection here. An amplifier with a big capacitor on its output is nice because it tends not to allow noise outside its bandwidth to sneak into the output. Here's a circuit I've used in the past:



With an ideal opamp, this circuit is critically damped for:

$$\texttt{c1} \to \frac{4\ \texttt{c2}\ \texttt{r2}\ \texttt{r3}}{(\texttt{r2} + \texttt{r3})^2}$$

In this case, its transfer function has two poles at:

$$s \to -\frac{r2 + r3}{2\, c2\, r2\, r3}$$

DC gain is just -r2/r1. For r2>>r3, the time constants are just 2 r3 c2. So, choose r3 to allow enough current drive, c2 to get the desired time constant. Then r2 can be as large as the bias current allows. Choose c1 to get critical damping by the formula above, and r1 to get the DC gain.

9/2/07 jpd Modularization and Sequencer

It's looking like 100-200 cm^2 of board space for the drivers, 300-500 cm^2 for an AE. It depends on the amount of independent clocking we want to do. Right now, the design I have assumes we'll clock all sections of the chip together. The flexprints allow some independence, but they are different for the P and N channel chips, so if we want to be able to clock sections independently I need to know what the requirements are. Do I need to support the independent clocking that the flexprints allow?

There's a simple 32 bit sequencer that Frank Larosa and I designed for MIT a few years ago. A few weeks ago, I talked to Frank about it, and he agreed to publish the FPGA design for it. The specification is at http://www.noqsi.com/images/SeqSpec.rtfd.pdf. It's a one-level sequencer, so it needs a computer to control it. I use one of these sequencers for testing driver designs.

For laboratory use, we could control the sequencer with a Linux PC, or we could put a microcontroller in the AE.

For digital video out, I'd like to use Camera Link because we can buy the interface boards and use published software. That might mean we want a microcontroller in the AE anyway (perhaps something like an ARM7).

Right now, I'm thinking of an AE of perhaps two boards for drivers, one sequencer, one video, and one interface. All except perhaps one of these boards will use the same design for P and N channel CCD's: I'm still considering whether one of the driver boards should use a common design. I'm planning for each board to be ~70 cm^2, but I'll reconsider this when I get more details worked out.

For digital to analog converters to set drive voltages, I see two possible ways to proceed: we can use commercial CMOS devices or serial delta-sigma DACs in FPGAs. The main reason to prefer the FPGA implementation is radiation tolerance: there's most likely no problem with the commercial CMOS, but we'd want to test it.

9/10/07 Back Bias

The P channel device needs up to +50V of back bias. The easiest way to get this may be a Cockroft-Walton voltage multiplier. There's an interesting writeup on optimizing these at http://blazelabs.com/e-exp15.asp. For ±12V drive, 3-4 stages are "optimum", and for 100 μA, 60V out, 1 MHz rate, only ~180pF capacitors are required according to their formulae. Some losses are to be expected, so go with 220pF capacitors. Note that the low capacitance helps in fault conditions, limiting the current. Use PMBTA42 transistors as HV regulator, common base level translator from opamp driving common emitter pass stage.

9/12/07 Some decisions

Can't study forever: have to get the design going. This is the preprototype phase: we'll have plenty of opportunity for change.

I'm going to try to design a universal driver board with enough resources to clock either kind of CCD. Otherwise minimalist: clock all sections together.

There will have to be different backplanes for P and N CCD's, because the interconnections are different. Drivers get different voltages. Zeners on each backplane can limit voltages to the different safe levels for each type, preventing costly mistakes. All drivers have current limits, so this should work.

Output drain drivers will go on video board, for noise and because right now it looks less crowded than the driver board.

CMOS DACs will set voltage levels, so we don't have to think about a serial FPGA DAC right now.

9/21/07

One change I'm making is retiring the old OP220 opamps in favor of OP490's. Better output current drive is the main reason, but lower power also helps.

9/29/07 Driver Board first Release

Maybe I should call this the "Gate Driver Board": I'm currently planning to put the various drain drivers and "vertical input source" driver on the "video" board.

There is no digital logic on this board: the "sequencer" and "controller" boards will provide the necessary digital inputs.

There are almost 400 components with almost 1200 connections on this board. This is about the same count as the HETE CCD "driver" board. That board, designed in 1992, was ~300 cm^2. The majority of the components on it were not surface mount devices, while the only "through hole" device in this design is the connector, J1. So, it seems to me that 100-150 cm^2 of board area should be adequate for this design.

My experience suggests that the driver board is usually the most crowded one in these systems, so whatever we decide for board size here should suffice for the other boards in the system. That's one reason why I designed this board first.

The board provides the following clocks, with high levels adjustable 0-10V and low levels adjustable -10V-0. These should be sufficient to clock either our P channel or N channel CCD with all sections operating synchronously.

P1VI
P2VI
P3VI

These are the vertical imaging area clocks.

P1VS
P2VS
P3VS

These are the vertical storage area clocks.

P1H
P2H
P3H
P4H

These are the horizontal clocks.

TG
SG
RG

Transfer gate, summing gate, reset gate.

The board also provides the following DC biases:

OG
IG1
IG2

Output and input gates, range -10V to 10V.

BB

P-channel back bias, range 0-50V.

J1 provides power and inputs to the board, and delivers its outputs to the AE

backplane.

Pin	Name	Function
A1	Gnd	
A2	+5	Logic and low voltage power
B3	Gnd	
A4	HP1VI	Logic: drive P1V1 high
B4	HP1VS	Logic: drive P1VS high
A5	LP1VI	Logic: drive P1V1 low
B5	LP1VS	Logic: drive P1VS low
A6	HP2VI	Logic: drive P2VI high
B6	HP2VS	Logic: drive P2VS high
A7	LP2VI	Logic: drive P2VI low
B7	LP2VS	Logic: drive P2VS low
A8	HP3VI	Logic: drive P3VI high
B8	HP3VS	Logic: drive P3VS high
A9	LP3VI	Logic: drive P3VI low
B9	LP3VS	Logic: drive P3VS low
A10	SP1H	Logic: drive P1H
B10	SP3H	Logic: drive P3H
A11	SP2H	Logic: drive P2H
B11	SP4H	Logic: drive P4H
A12	Gnd	
B12	1MHz	Logic: 1MHz clock
A13	DCK	Logic: DAC data clock
B13	DS0/	Logic: Select DACs 0-7
A14	DS8/	Logic: Select DACs 8-15
B14	DD	Logic: DAC serial data
B16	Gnd	
A17	AHK	Analog housekeeping bus
A18	HA0	Logic: housekeeping address bit 0 (LSB)
B18	HA2	Logic: housekeeping address bit 2
A19	HA1	Logic: housekeeping address bit 1
B19	HEN16	Logic: enable housekeeping channels 0-7
A20	HEN8	Logic: enable housekeeping channels 8-15
B20	HEN0	Logic: enable housekeeping channels 16-23
A21	Gnd	
A22	SSG	Logic: drive SG
B22	STG	Logic: drive TG
A23	SRG	Logic: drive RG
A30	Gnd	
B38	IG1	Bias out to IG1
A39	IG2	Bias out to IG2
B39	OG	Bias out to OG
A40	Gnd	
B40	P1VI	Clock out to P1VI

A41	P2VI	Clock out to P2VI
B41	P3VI	Clock out to P3VI
A42	P1VS	Clock out to P1VS
B42	P2VS	Clock out to P2VS
A43	P3VS	Clock out to P3VS
B43	P1H	Clock out to P1H
A44	P2H	Clock out to P2H
B44	P3H	Clock out to P3H
A45	P4H	Clock out to P4H
B45	TG	Clock out to TG
A46	SG	Clock out to SG
B46	RG	Clock out to RG
A47	Gnd	
A48	BB	Back bias out
A49	+12	Driver power
B49	Gnd	
A50	-12	Driver power

Board details:

drivers.1.sch and drivers.2.sch

These are the parallel clock drivers, composed mainly of subcircuits (details in other drawings).

Resistors R1-R4 isolate the high impedance housekeeping system from the voltages it measures. Similar 100k resistors are present on all housekeeping test points on the board.

ParallelDriver.sch

This is the high curent/high voltage driver for the parallel clocks. Vps is a high current input at the clock high level, nominally 0-10V DC. Vpg is gate drive power for the P channel switch, nominally 5V below Vps. Vns and Vng are similar for the N-channel negative level, nominally -10V-0.

GoHi drives the output high when asserted to logic high. GoLo drives the output low when asserted to logic high.

R6 and R7 are "brute force" current limiters: they protect Q1 and Q2 against latchup of U1, sequencer microcode errors, and output short circuits. They also dissipate the bulk of the capacitive switching energy, keeping the transistors cool. I suggest Ohmite TDH35P5R00JE, rated at 35W at 25C case temperature. Whether this is sufficient needs attention: for example, a latchup or microcode error could turn on both Q1 and Q2, allowing as much as 1.8A (the LM317 regulator's current limit) to flow. That's 16W per resistor. Short circuit is worse: the LM337 on the negative

supply has a higher limit (3.7A). But, I don't know what the power supply will provide, and I don't know what we consider "worst case". I believe in most cases the regulators will thermally limit before the resistors overheat, but that depends on clock voltage settings. Clever layout could help (put the regulator chips where the resistor heat will put them into thermal shutdown). I think this is good for a lab prototype, but for flight we may want thermistors and a shutdown circuit.

The 300 ohm resistors are latchup protection for U1: they're 1W SMT (2512). 12V power limits their dissipation to <0.5W. However, they only limit current to 40 mA, exceeding the 20-30 mA limits (depending on manufacturer) of U1. It's not clear that those limits apply to latchup conditions, though. Increasing the resistance will slow the driver down, but perhaps that's acceptable. Another thing to consider in the flight design, after we get some lab experience.

ParallelRegs.sch

In this design, I've chosen to use LM317/337 regulators for their ruggedness. Their current limiting should be effective protection against short circuits, and help protect against latchup too. They're not as efficient as some more modern designs, so if we need to trim some power we can revisit this choice.

DACtoClock.sch

This circuit translates 0 to 3.3V DAC outputs to 8.75 to -1.25V (for 10V to 0 clock high levels) and 1.25 to -8.75V (for 0 to -10V clock low levels), compensating for the 1.25V offset of the voltage regulator chips.

drivers.3.sch and drivers.4.sch

These are the low capacitance clock drivers.

TG, SG, and RG drivers are just doubled-up serial clock drivers. We could save a few parts by making up a single channel driver subcircuit.

SerialDrivers.sch

See above about 300 ohm limiting resistors.

drivers.5.sch

This is the high voltage generator and regulator for the 12-50V back bias.

I had previously chosen 220 pF as optimum for C1-C6, but upon more reflection, it's silly to optimize this circuit for minimum capacitance. Increasing the capacitance in the Cockroft Walton circuit will decrease the ripple without significant cost. We can get 47nF 50V in an 0603 package. Leave C4 at 220 pF to limit current under short

circuit conditions. The maximum dissipation in the DG403 will then be f*C*V^2, or 127 mW for 24V swing, 1 MHz.

drivers.6.sch

These are just simple filtered amplifiers to convert 0 to 3.3V DAC outputs to 10V to -10V low current biases.

drivers.7.sch

A pair of AD5308 octal DAC chips provide the 16 control voltages required for the drivers. Note that the regulators invert, so a code of 0xff sets the corresponding driver voltage to its most negative, while a code of 0x00 sets it to the most positive.

drivers.8.sch

These are the housekeeping multiplexors. As on ASCA and Suzaku, the approach is to feed an analog voltage to a line on the backplane. An ADC on the "controller" board will handle housekeeping.