Designer's notebook for TES CCD System Analog Electronics

7/27/07 Packaging and modularization

Funny not to be starting from noise, but photon shot noise (hundreds of counts RMS) is much larger for this design than I'm used to (and other noise may even dominate the big image stacks we intend to use), and Vince Deno is charging ahead on the systems engineering, so I'll start with modularization.

I think the systems we built at MIT in the 80's and 90's showed that a mother/daughter board approach with about 100 contacts on each daughter is a comfortable modularization. "Rent's Rule" of scaling then tells you to expect ~1000 internal connections on each board, and that's about what we got. Looking at things we've done recently, it seems we can get something like 16 connections/cm^2 with COTS surface mount parts without working too hard. So 1000 connections takes about 60 cm^2. Leave some room around the edges, go with 6x12 cm boards. About 1/4 the area of a HETE "Lasagna Box" board, but it's been 15 years since I designed those: quadrupling the parts density isn't so ambitious. The HETE boards were nice and stiff, so these should be even better (square-cube law).

Higher density boards need higher density connectors. We used 100 mil pitch 3 row 96 pin DIN connectors in the HETE era. I'm looking to use 50 mil pitch 100 pin Hirose FX2 series here. Rated to -55C, available from Digi-Key. These are 7.5 mm high. Assume 2 mm board, 2 mm for backside components, 1 mm clearance, we get a board pitch of 12.5 mm, not bad. We intend to run the camera assembly as cold as possible, so a cold rated connector is good.

Tentative board list, per camera:

1   Power/thermal control
1   Cameralink interface
1   Sequencer   (repackaged EDCCD sequencer)
2   Driver (might be only one)
2   Video (or could be hybridized with focal plane)

If we add in fast chips for ACS, might need a couple more. Still, the whole thing will be less than half the volume of a HETE "lasagna box" while supporting twice as many video streams each with 20 times the pixel rate.

7/30/07

CCD clock drivers

Each planned focal plane is four 2k by 2k three phase chips with 15 μm pixels (modified Lincoln Lab CCID-20). 36 cm^2 of sensitive area. At 5 nF/cm^2 for each phase, we have 180 nF of capacitive load on each driver, assuming we clock the chips together. Frame store clocks are the same.

Experiments with TC1411 chips have shown how nice these are for driving large capacitances. Select those. Choose a fixed 5V swing: we know from experiments at MIT that this is fine with this pixel design.

This choice suggests we should have a substrate potential above system ground, since the TC1411's low output voltage needs to be very near its logic low voltage. Parallel low is generally the lowest voltage in the system, so we'll have all positive supplies in the analog electronics. Right now I'm looking at:

+3.3V   DAC, ADC, analog signal processing
+5V   Parallel clocks
+12V   Serial/reset clocks
+30V   Biases, on-chip charge amplifiers

There's also digital: maybe 3.3V and 2.5V there, but that's down the road.

MAX4593 seems a good choice for serial/reset clock driving.

Clock Drivers:

Parallel IA (3)
Parallel FS (3)
Serial (3)
Reset gate (1)

Clock DACs:

Serial (2)
Reset gate (2)

Bias Drivers (each with a DAC):

Output gate (1)
Scupper (1)
Reset drain (1)
Substrate (1)

Output drain (16)

Total outputs from drivers to focal plane: 30
Total sequencer bits: 10
Total DACs: 24

8/8/07 Driver board

See www.noqsi.com/images/fastreg-model.zip for serial clock regulator model. This is critical to a flat, stable bias.

See www.noqsi.com/images/SXI-Notebook-20070620.pdf for bias/reset clock regulator model (from NeXT SXI development).

See www.noqsi.com/images/TESS_drivers.zip for driver board schematics (incomplete).

Tentative capabilities:

Parallel drive fixed at 0-5V relative to system ground.
Serial low 0-8V relative to system ground.
Serial high 3-11V relative to system ground.
Reset low, high 6-11V relative to system ground.

Are these enough? If not, what are requirements?